Page 26, strike all of line 4, and substitute the following therefore: -Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned,-.

IN THE CLAIMS:

Amend the following claims as indicated:

1 ~~63~~. (Amended) A method of operating [with a host processor] a bulk storage memory with a host processor, wherein the bulk storage memory includes [including] an array of non-volatile floating gate memory cells, comprising:

storing, within defined non-overlapping groups of array cells, sectors of user data and associated overhead data, said overhead data being generated within the bulk storage memory to include [containing] information either of the individual memory array cell groups in which the overhead data are stored or of the user data stored in the same memory array cell groups as the overhead data,

in response to receipt from the host processor of an address in a format designating at least one mass memory storage block address, converting said at least one mass memory storage block address into an address of at least one of the memory array cell groups and addressing said at least one of the memory array cell groups,

in response to receipt from the host processor of user data and a command to write said user data to said at least one mass memory storage block address, writing [at least one sector of] said user data [and associated overhead data] into the addressed at least one of the memory array cell groups, and

in response to receipt from the host processor of a command to read user data from said at least one mass memory storage block address, reading at least one sector of said user data and ~~associated~~ overhead data from the addressed ~~at least one of the memory array cell groups~~.

2 ~~64~~. (Amended) The method according to claim 63, wherein, in response to receipt from the host processor of [a] the command to write user data, [first] reading and processing the overhead data [associated with the user data] stored in the addressed at least one of the groups of array cells prior to writing the user data into said addressed at least one of the groups of array cells.

4 ~~66~~. (Amended) The method according to any one of claims 1 ~~63~~-3 ~~66~~, wherein the overhead data stored within the addressed at least one of the groups of array cells includes the address of [said at least one group] the group in which the overhead data are stored.

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33 ~~83.~~ (Amended) The memory system according to claim ~~82~~ 32 additionally comprising a list of any [unusable ones] of said designated locations that are unusable [to] that link said unusable locations with others of said locations that are usable, and wherein said addressing circuit includes a circuit to access linked others of said locations in place of said unusable locations.

34 ~~84.~~ (Amended) The memory system according to claim ~~83~~ 33 wherein the list of unusable locations includes a list maintained within the bulk storage memory system outside of locations of the memory array designated to store blocks of user data and associated units of overhead data.

35 ~~85.~~ (Amended) The memory system according to claim ~~83~~ 33 wherein the list of unusable locations includes a list stored as part of units of overhead data associated with unusable locations of the memory array.

36 ~~86.~~ (Amended) The memory system according to any one of claims ~~83-85~~ 33 35 wherein the list of any unusable locations includes inoperable or defective locations.

37 ~~87.~~ (Amended) The memory system according to any one of claims ~~83-85~~ 33 35 wherein the list of any unusable locations includes locations that contain a number of defective cells ~~in excess of a preset number.~~

38 ~~88.~~ (Amended) The memory system according to any one of claims ~~82-85~~ 32 35 wherein said given amount of user data is substantially 512 bytes.

39 ~~89.~~ (Amended) The memory system according to any one of claims ~~82-85~~ 32 35 wherein said mass memory storage block address is a magnetic disk sector address.

40 ~~90.~~ (Amended) The memory system according to claim ~~89~~ 39 wherein said magnetic disk sector address includes a head, cylinder and sector.

43 ~~91.~~ (Amended) The memory system according to any one of claims ~~82-85~~, 32 35 wherein said bulk storage memory system is implemented in a single package.

44 ~~92.~~ (Amended) The memory system according to claim ~~91~~ 43, wherein said bulk storage memory system is provided within a card that is removably connectable to the computer system through an electrical connector.

C5 Amend 47 ~~93.~~ (Amended) The memory system according to any one of claims ~~82-85~~ 32-35, wherein individual blocks of user data and corresponding units of overhead data are stored together within individual ones of a plurality of locations of the memory cell array.

48 ~~94.~~ (Amended) The memory system according to claim ~~93~~ 47, additionally comprising an erasing circuit [to] that simultaneously [erasing] erases the individual cells within individual designated locations to simultaneously erase any user data and associated unit of overhead data stored ~~therein~~.

Add the following new claims:

30 --~~95~~. The method according to any one of claims ~~63-65~~ 1-3 and ~~67-71~~ 7-11, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

5 ~~10~~ ~~96~~. The method according to claim ~~66~~ 4, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

C6 14 ~~14~~ ~~97~~. The method according to claim ~~72~~ 12, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

20 ~~15~~ ~~20~~ ~~98~~. The method according to claim ~~74~~ 16, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

24 ~~99~~. The method according to claim ~~71~~ 23, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

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28 ~~100.~~ 26 The method according to claim ~~78~~, wherein storing data includes programming the individual memory cells of the array into one of exactly two programmable states in order to store exactly one bit of data per cell.

31 ~~101.~~ 1-3 or 7-11 ~~4-8~~ ~~19-21~~ The method according to any one of claims ~~63-65~~ and ~~67-71~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

6 ~~11~~ ~~102.~~ 4 ~~9~~ The method according to claim ~~66~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

15 ~~10~~ ~~15~~ ~~103.~~ ~~9~~ ~~12~~ 12 The method according to claim ~~72~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

21 ~~16~~ ~~21~~ ~~104.~~ ~~11~~ ~~16~~ 16 The method according to claim ~~74~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

25 ~~105.~~ 23 The method according to claim ~~77~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

29 ~~106.~~ 26 The method according to claim ~~78~~, wherein storing data includes programming the individual memory cells of the array into one of more than two programmable states in order to store more than one bit of data per cell.

51 ~~107.~~ 32 35 The memory system according to any one of claims ~~82-85~~, wherein the cells of the array are individually programmable into exactly two states in order to store exactly one bit of data per cell.

41 ~~108.~~ 39 The memory system according to claim ~~89~~, wherein the cells of the array are individually programmable into exactly two states in order to store exactly one bit of data per cell.

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45 ~~109.~~ The memory system according to claim 44 ~~92~~, wherein the cells of the array are individually programmable into exactly two states in order to store exactly one bit of data per cell.

49 ~~110.~~ The memory system according to claim 48 ~~94~~, wherein the cells of the array are individually programmable into exactly two states in order to store exactly one bit of data per cell.

52 ~~111.~~ The memory system according to any one of claims 32 ~~82~~-35 ~~85~~, wherein the cells of the array are individually programmable into more than two states in order to store more than one bit of data per cell.

42 ~~112.~~ The memory system according to claim 39 ~~89~~, wherein the cells of the array are individually programmable into more than two states in order to store more than one bit of data per cell.

46 ~~113.~~ The memory system according to claim 44 ~~92~~, wherein the cells of the array are individually programmable into more than two states in order to store more than one bit of data per cell.

50 ~~114.~~ The memory system according to claim 48 ~~94~~, wherein the cells of the array are individually programmable into more than two states in order to store more than one bit of data per cell.

53 ~~115.~~ A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and linking the addresses of such unusable sectors with addresses of other sectors that are useable,

causing the controller, in response to receipt from the processor of an address in a format designating at least one magnetic disk sector, to generate an address of a non-volatile memory sector that corresponds to said at least one magnetic disk sector,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the linked address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector,

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of said accessed useful sector, and

wherein writing to the accessed usable sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one ~~bit of data or information~~ per cell.

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54 ~~116~~. The method according to claim 53 ~~115~~, wherein the detecting of the predefined condition includes detecting when individual sectors become defective.

55 ~~117~~. The method according to claim 54 ~~116~~, wherein the detecting of when individual sectors become defective includes determining when a number of individual defective memory cells within a sector exceed a given number.

56 ~~118~~. The method according to claim 53 ~~115~~, wherein the user data portion of the individual non-volatile memory sectors has a capacity of substantially 512 bytes.

57 ~~119~~. The method according to claim 53 ~~115~~, wherein the information stored in the overhead portion of the individual sectors includes an address of the respective ones of the individual sectors.

58 ~~120~~. The method according to claim 53 ~~115~~, wherein the information stored in the overhead portion of the individual sectors includes an error correction code calculated from data stored in the user data portions of corresponding ones of the individual sectors.

59 ~~121~~. The method according to claim 53 ~~115~~ wherein linking the address of unusable sectors with sectors that are useable includes maintaining a list within the card that links such

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unusable sectors with addresses of corresponding ones of the other sectors that are useable, and wherein accessing a usable sector includes referring to the list to translate the address of the unusable sector into an address of a usable sector.

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122. The method according to claim 115 wherein linking the address of such unusable sectors includes storing within individual ones of the defective sectors addresses of corresponding useable sectors, and wherein accessing a usable sector corresponding to an unusable sector includes referring to the useable sector address stored in the unusable sector.

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123. The method according to claim 115, wherein causing the controller to generate an address of a non-volatile memory sector includes doing so for a non-volatile memory sector that corresponds to only one magnetic disk sector, wherein the user data portion of the individual non-volatile memory sectors has a capacity that is substantially the same as a user data portion of said one magnetic disk sector.

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124. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of an address in a format designating at least one magnetic disk sector, to designate an address of at least one non-volatile memory sector that corresponds with said at least one magnetic disk sector,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector,

either writing to, or reading from, said overhead portion of said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector, and

wherein writing to said at least one non-volatile memory sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store ~~more than one bit of data~~ per cell.